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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,780	07/24/2001	Taketoshi Nakano	70840-56281	3887

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Dike, Bronstein, Roberts & Cushman
Intellectual Property Practice Group
Edwards & Angell
P.O. Box 9169
Boston, MA 02209

EXAMINER
LESPERANCE, JEAN E

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,780	NAKANO ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-7 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U.S.C. 102 (b) as being unpatentable over U.S. Patent # 6,025,822 ("Motegi et al.).

As for claim 1, Motegi et al. teach a row generating data Fig.4 (41) corresponding to a data input section for receiving a control data signal for the plurality of column electrodes; a latch circuit includes a timer Fig.4 (16) corresponding to a timing control section for generating a timing control signal for controlling at least one of the row electrode driving circuit and the column electrode driving circuit; a selection data section (Fig.4) corresponding to a selection section for selecting one of a signal in synchronization with the timing signal generated by the timing control section and the control data signal input to the data input section, based on the control data signal input to the data input section; and memory unit (10) corresponding to a data output section for outputting one of the signal in synchronization with the timing signal and the control data signal which is selected by the selection section, wherein the data input section of

a second column electrode driving circuit of the plurality of column electrode driving circuits is connected to the data output section of a first column electrode driving circuit of the plurality of column electrode driving circuits, and the liquid crystal driving circuit (14) corresponding to the data output section of the second column electrode driving circuit is connected to the data input section of a third column electrode driving circuit of the plurality of column electrode driving circuits.

As for claim 2, Motegi et al. teach an integrated circuit column drivers Fig.7 (21) which are connected in series with the other circuits includes a data input from the controller and each of the circuit includes a level shifter circuit which embedded a timer circuit corresponding to the data input section of the second column electrode driving circuit includes an external data input port for receiving an external control data signal and a transferred data input port for receiving a control data signal from the first column electrode driving circuit, the external data input port and the transferred data input port being switchable, and the timing control section of the second column electrode driving circuit is switchable to an operation state or a non-operation state in accordance with the switching between the external data input port and the transferred data input port.

As for claim 3, Motegi et al. teach an integrated circuit column drivers Fig.7 (21) which are connected in series with the other circuits includes a data input from the controller and each of the circuit includes a level shifter circuit which embedded a timer circuit corresponding to the data input section of the second column electrode driving circuit receives one of the external data signal and the control data signal from the first column electrode driving circuit which is selectively input thereto, and the timing control

section of the second column electrode driving circuit is switchable to an operation state or a non-operation state by the external control data signal.

As for claim 4, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits on the display panel; and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits provided on the display panel, wherein: column drivers 21 are connected in series Fig.7 (21) and are transferred in cascading manner corresponding to the plurality of column electrode driving circuits are connected in series along a first side of the display panel, so that a scanning signal from the first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, is transferred in a cascading manner in the plurality of column electrode driving circuits, row drivers Fig.7 (22) are connected in series and are cascading with each other corresponding to the plurality of row electrode driving circuits are connected in series along a second side of the display panel adjacent to the first side, so that the scanning signal from the first column electrode driving circuit is transferred in a cascading manner in the plurality of row electrode driving circuits, an external control data signal is input to the data input section of the first column electrode driving circuit and is output in synchronization with a timing signal generated by the timing control section of the first column electrode driving circuit, controller Fig.4 (2) corresponding to the external control data signal which is output from the first column electrode driving circuit is transferred sequentially in the rest of the plurality of column

electrode driving circuits in a cascading manner, and the timing signal is transferred sequentially in the plurality of row electrode driving circuits in a cascading manner as the scanning signal.

As for claim 5, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits arranged in a line and provided along a first side of the display panel; and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side, wherein: controller Fig.1 (2) a control data signal for driving the display panel is input to a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, a level shifter circuit Fig.1 (14b) includes a timer corresponding to a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits is generated in the first column electrode driving circuit, and the generated timing signal and a data signal are output to a second column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the first column electrode driving circuit, the output data signal is transferred to a third column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the second column electrode driving circuit, and the generated timing signal is transferred in

a cascading manner to the plurality of row electrode driving circuits as a scanning signal.

As for claim 6, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits arranged in a line on a printed circuit board provided along a first side of the display panel (it is inherent for the semiconductor integrated circuit to include a printed circuit board); and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side, wherein: a controller Fig.1 (2) includes all of the circuits before going to the display panel (TCP) corresponding to each of the plurality of column electrode driving circuits is mounted in a tape carrier package, a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and controller Fig.6 (2) includes all the components before outputting to display panel (TCP) corresponding to the plurality of row electrode driving circuits, and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuits, which is closest to the first column electrode driving circuit as a scanning signal, a timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through a first line portion provided on the tape carrier package mounting the first column electrode driving

circuit, a second line portion provided on the printed circuit board, a third line portion provided on the tape carrier package mounting the first column electrode driving circuit, and a fourth line portion provided on the display panel.

As for claim 7, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits arranged in a line on a printed circuit board provided along a first side of the display panel (it is inherent for the semiconductor integrated circuit to include a printed circuit board); and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side, a controller Fig.7 (23) is to write input display data in a RAM 24 once and to supply control signals to the column drivers 21 and row drivers 22 through control signal lines 25, 26 (column 1, lines 51-53) corresponding to a timing signal for controlling the plurality of row electrode driving circuits is supplied to one of the plurality of row electrode driving circuits sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between

8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 3-10-2003

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600